

MPPA[®] 3 Coolidge™

Intelligent Data Processing, From Cloud to Edge

APPLICATIONS



Data Centers



Autonomous Vehicles



Video Surveillance



Aerospace & Robotics



Industry 4.0



5G Telecom Infrastructure

KEY BENEFITS



Power efficiency/ High performance computing



AI acceleration



Very high-speed interfaces

PCIe Gen4 x 16,
2 x 100G Ethernet



Real-time data processing



Parallel execution of multiple critical tasks



Standard programming

C/C++/Open standards,
Linux, POSIX, RTOS



Security/Safety

Determinism, freedom of interference, secure boot

■ **Learn more:**

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Taking full advantage of Kalray's patented MPPA[®] (Massively Parallel Processor Array) architecture and 16nm FinFet technology, Coolidge™ is a scalable 80-core processor designed for intelligent systems. **It offers a compelling alternative to GPU, ASIC and FPGA, bringing unique value to multiple applications from Data Centers, to Edge or Embedded systems.**



Kalray software development kit, relying on standard tools and Application Programming Interface (APIs), enables seamless port of existing applications or easy development of new ones.

Develop Next Gen Storage and Networking Systems

- **Flexible integration in state-of-the-art PCIe Gen4, 100GbE appliances**
 - JBOF Target controller, I/O controller, SmartNIC, SmartSSD use cases
 - 2 configurations: stand-alone or x86 CPU offloading
 - Support virtualized, containerized or bare metal infrastructures
 - Dynamic resource allocation for Control, Data & Management Planes
- **Acceleration of high-performance protocols, services and QoS**
 - NVMe-oF, RoCE/RDMA, TCP/IP, NVMe, OVS/NFV protocols
 - Smart Load-Balancer, Priority Flow Control, Stateless L1-L4 parsing
 - RAID6: 154 Gbit/s Erasure Coding (Reed-Solomon) per cluster
 - Line-rate encryption/decryption/hash (IPSEC, TLS, XTS, MACsec)
 - AI capability for analytics and adaptive configuration

Build Accelerated Compute-Intensive Applications

- **Acceleration of complex workloads**
 - Patented core + co-processor boosting Machine Learning Inference
 - Computer Vision
 - Signal Processing (e.g. FFT), Cryptography, Mathematics
- **Build stand-alone intelligent embedded systems**
 - Multi-OS (Linux, RTOS) systems
 - Support "Freedom from Interference" for mix criticality
- **Build next gen Edge Computing Systems**
 - Process Data at the Intelligent Edge
 - Real-time analytics for automation, prediction, and control
 - Easy integration into existing systems

80-Cores Architecture

Core

- 64-bit/32-bit architecture
- From 600MHz to 1.2 GHz
- 6-issue VLIW
- 16KB instruction cache / 16KB data cache with MMU
- IEEE 754-2008 Floating Point Unit (FPU)
- Square root and reciprocal operations in floating single precision
- 64-bit integer multiplication (Asymmetric cryptography)
- Up to 4 execution rings
- Up to 256-bits per cycle Load/Store

Co-processor (one per Core)

- Acceleration of INT8, INT16 or FP16 accuracy
- Up to 128 MAC per cycle

Cluster

- 16 Application Cores + 1 Management/Security Core
- 4 MB of Memory / L2 Cache – 600GB/s Low Latency / High Speed
- Configurable cluster/chip cache coherency & deterministic modes

System-on-Chip

- 5 clusters (total of 80 Application Cores + 5 Management Cores)
- Up to 1.15 TFLOPs (SP) / 384 GFLOPs (DP)
- Up to 3 TFLOPs (16 bits) / 25 TOPs (8bits) for deep learning
- 56GB/s chip-to-chip communications (16 +12.5) x 2

PCIe Gen4 Interface

- 16-lane PCIe GEN4 Endpoint (EP) or Root Complex (RC)
- Bifurcation up to 8 downstream ports in RC mode
- SR-IOV up to 8 Physical Functions / 248 Virtual Functions
- Address translation and protection
- Up to 2048 MSI-X & 64 MSI interrupts
- Support for Hot Plug
- Up to 512 DMAs for multi queues / kernel bypass drivers
- Direct PCIe-to-clusters and PCIe-to-DDR transfers
- Support for NVMe and VIRTIO emulation

LPDDR4/DDR4 Interface

- 64-bit DDR4/LPDDR4-3200 channels with sideband/inline ECC
- Up to two ranks per DDR4 Channel
- 2 DDR channels (up to 32GB) with channel interleaving

2x100GbE Ethernet Interface

- 8x1/8x10/8x25/2x40/4x50/2x100 GbE
- RDMA over Converged Ethernet (RoCE v1 and v2)
- Jumbo Frame Support (9.6KB)
- Support for PTP/IEEE 1588v2
- Priority Flow Control (PFC), IEEE 802.1Qbb
- Checksum offload Header & Payload
- Line rate packet classification/smart load balancing
- Hash & Round-robin based dispatch policy

Security

- Secure Boot with authentication & encryption
- True Random Number Generators (TRNG)
- RSA, Diffie-Hellman, DSA, ECC, EC-DSA and EC-DH acceleration

Cryptography Accelerators (optional)

- AES-128/192/256 (ECB/CBC/ICM/CTR/GCM/GMAC/CCM)
- AES-XTS for storage application
- MD5/SHA-1, SHA-2, SHA-3
- Kazumi/Snow 3G, ZUC

Management/Control Interfaces

- GPIOs/UARTs/SPI/I2C/CAN/PWM
- SSI Controller for serial NOR Flash with optional boot
- SDCARD UHS-I / eMMC 4.51 memory controller
- 2x USB 2.0 OTG ULPI
- JTAG IEEE 1149.1
- 16-bit Parallel Trace Interface

Safety & Predictability

- Mix criticality support
- Lockable critical configuration
- Capability to bank memory and caches for non-interference & time-predictable execution
- L1 Cache coherency enabling/disabling

MPPA®3 Coolidge™ Processor Block Diagram

Coolidge™ is composed of 5 clusters with 16 cores dedicated to applications and 1 core for management and security each.

Need more performance?

Connect several MPPA® processors together to reach the level of performance you need.

